**UNITED STATES DEPARTMENT OF COMMERCE**
**Patent and Trademark Office**
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| | | | |

| EXAMINER | |
|---|---|
| ART UNIT | PAPER NUMBER |
| | 2 |

**DATE MAILED:**

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. 09/405,945 | Applicant(s) Bo Jin et al. |
|---|---|---|
| | Examiner Lynette T. Umez-Eronini | Group Art Unit 1765 |

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claims**

☒ Claim(s) *1-20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

**Application Papers**

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

*--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---*

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 5, the phrase, "a first insulating" is indefinite because it is unclear what is meant. It is assumed that insulating refers to "an insulation layer" which would be searched.

In claim 1, line 7, the phrase, "a contact hole etch stop layer" is indefinite because it is unclear what is meant.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (U. S. Patent No. 5,503,901) in view of Chang et al. (U.S. patent No. 5,893,740).

Sakai et al. teach a method comprising:

forming and etching an interlayer insulating film above an MOSFET to form a contact hole in a self alignment manner with respect to a gate electrode (column 9, line 58 - column 10, line 16), which reads on forming a contact hole through a first insulating that is self-aligned with respect to a transistor gate.

Sakai et al. do not expressly disclose a transistor gate length of less than 0. 2 microns.

In a method of forming an integrated circuit device, it is noted that a transistor comprises a gate electrode which is synonymous with the term, a transistor gate and Chang et al. teach forming a short channel field effect transistor having a gate electrode of less than 0.1 microns (column 1, line 5-7 and column 3, line 11-20), which reads on a transistor gate having a gate length less than 0.2 microns.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Sakai et al. by having a transistor with a gate length less than 0.2 microns as taught by Chang et al. to form a submicron semiconductor device.

5. Claims 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (U. S. Patent No. 5,503,901) in view of Chang et al. as applied to claim 1, and further in view of Nulty et al. (U. S. Patent No. 5,468,342).

Unlike claim 2, Sakai et al. in view of Chang et al. do not expressly teach forming a contact hole includes reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide.

In the art of fabricating semiconductor devices, Nulty et al. teach forming a contact hole by reactive plasma etching through a BPSG layer (column 1, line 14-25 and column 6, line 15-20).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Sakai et al. in view of Chang et al. by forming a contact hole include reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide as taught by Nulty et al. for the purpose of providing a region whereby contact is made between conductive layers or devices lying in or on a semiconductor substrate and layers overlying the substrate.

Unlike claim 4, Sakai et al. in view of Chang et al. do not expressly teach reactive plasma etching includes $CHF_3$ and $C_2H_4F_4$ and the flow rate of each of these etchants.

Nulty et al. teach reactive ion etching using $CHF_3$ and $C_2H_4F_4$ in a LAM 384T system using (column 7, line 4-13 and column 9, line 30-34), which reads on introducing $CHF_3$ and $C_2H_4F_4$ into an etch chamber.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Sakai et al. in view of Chang et al. by reactive plasma etching

with $CHF_3$ and $C_2H_4F_4$ into an etch chamber as taught by Nulty et al. for the purpose of providing a region whereby contact is made between conductive layers or devices lying in or on and layers overlying a semiconductor substrate.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (U. S. Patent No. 5,503,901) in view of Nulty et al. (U.S. patent No. 5,468,342).

Sakai et al. teach a method comprising:

etching an interlayer insulating film above an MOSFET to form a contact hole in a self alignment manner with respect to a gate electrode (column 10, line 2-6 and Figure 20), having silicon nitride side walls (column 9, line 64 and 65), and having a SiO2/SiN selectivity or 20 or more (column 12, line 10 and 11; column 2, line 19 and 20; and Figure 20), which reads on etching a contact hole through a first insulating layer that is self-aligned with respect to a conductive structure having insulating sidewalls with an etch selectivity between the first insulating layer and the sidewall than is greater than ten to one.

Sakai et al. do not expressly disclose etching a contact hole through a first insulating layer comprising doped silicon dioxide.

In the art of fabricating semiconductor devices, Nulty et al. teach etching a contact hole through an oxide layer such as doped silicon dioxide (column 1, line 14-25).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Sakai (U. S. Patent No. 5,503,901) in view of Chang et al. by forming a contact hole through a first insulating layer comprising doped silicon dioxide as taught by Nulty et al. for the purpose of providing a region whereby contact is made between conductive layers or devices that lie in or on a semiconductor substrate and layers overlying the substrate.

6. Claim 13-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (U. S. Patent No. 5,503,901) in view of Nulty et al. (U.S. patent No. 5,468,342) as applied to claim 12.

Unlike claim 16, Sakai et al. do not expressly teach forming a hard mask comprising an insulating material over the first insulating layer; and forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask.

In the method of fabricating a semiconductor device, Nulty et al. teach forming a hard mask comprising an insulating layer over the first insulating layer (column 6, line 24-26) and forming contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard mask (column 4, lines 21, 22, and 44-54)

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Sakai et al. by forming a hard mask comprising an insulating layer over the first insulating layer and forming contact hole include etching through the first insulating layer with a selectivity between the first insulating layer and the hard mask as taught by Nulty et al. for the purpose of controlling the profile of the contact opening.

Unlike claim 17, Sakai et al. do not expressly teach the hard etch mask comprises silicon dioxide and the first insulating layer comprises phosphorous doped silicon dioxide.

In the art of etching semiconductor material, it is known that hard etch masks are made of conventional materials such as silicon dioxide and that insulating layers are made of conventional materials such as phosphorous doped silicon dioxide which inherently read

It would be inherent that by using conventional materials as described above, one would form a hard etch mask of silicon dioxide and an insulating layer of phosphorous doped silicon dioxide for the purpose of forming layers on the semiconductor device.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Sakai (U. S. Patent No. 5,503,901).

Sakai teaches a method, comprising:

forming an interlayer insulating film above an MOSFET to form a contact hole in a self alignment manner with respect to a gate electrode (column 9, line 58 - column 10, line 16) and showing a silicon dioxide insulating layer, silicon nitride sidewalls and two polysilicon conducting structures that are separated by 300 nm (Figures **2b** and **20**), which reads on forming a contact hole through an insulating layer between conducting structures, having sidewalls, structures, wherein the insulating comprises silicon dioxide. The absence of a teaching of forming a protective liner over the conducting structures would inherently read on the limitation, without forming a protective liner over the conducting structures.

***Claim Rejections - 35 USC § 103***

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (U. S. Patent No. 5,503,901) as applied to claim 18, in view of Woodruff et al. (U.S. patent No. 5,037,781).

Unlike claim 19, Sakai does not expressly disclose the insulating layer comprises silicon dioxide having a concentration of phosphorus dopants greater than 5% by weight.

In the art of fabricating semiconductor devices, Woodruff et al. teach an oxide layer that is BSPG with a phosphorous concentration by weight ranging from 1% to 8% (column 2, line 27 -32).

It would have been obvious to one having ordinary skill in the art at the time of the e claimed invention to modify Sakai et al. by using an oxide layer having a phosphorous dopant that is greater than 5% by weight as taught by Woodruff et al. for the purpose of providing a region whereby contact is made between conductive layers or devices that lie in or on and layers overlying a semiconductor substrate.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (U. S. Patent No. 5,503,901) as applied to claim 18.

Unlike claim 20, Sakai et al. do not expressly teach forming a hard mask comprising substantially undoped silicate glass over the first insulating layer, wherein the hard mask having openings over a contact hole location.

In the method of forming contact holes in semiconductor devices, it is well known to form a hard mask made of conventional materials such as undoped silicate glass which overlies an insulating layer wherein the mask has openings over a contact hole location.

It would have been obvious to use conventional materials and methods to form a hard mask comprising substantially undoped silicate glass over the first insulating layer,

wherein the hard mask having openings over a contact hole location for the purpose of improving the etch selectivity of the underlying insulating layer.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is (703) 306-9074.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

ltue

September 21, 2000